REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Office Action of December 4, 2002 has been received and contents carefully reviewed.

By the present amendment, Applicants hereby amend claim 8 and cancel claim 7 without prejudice. Accordingly, Applicants respectfully submit claims 1-6 and 8-14 remain pending within the present application.

In the Office Action of December 4, 2002, the Examiner rejected claims 1-11 and 15-17 under 35 U.S.C. §102(b) as being anticipated by Matsuo et al. (U.S. Pat. No. 4,319,237); and rejected claims 12-14 under 35 U.S.C. §103(a) as being unpatentable over Matsuo et al. in view of Berting et al. (U.S. Pat. No. 4,393,379). The rejections of these claims is traversed and reconsideration of the claims is respectfully requested in view of the following remarks.

The rejection of claims 1-11 and 15-17 under 35 U.S.C. §102(b) as being anticipated by Matsuo et al. is respectfully traversed and reconsideration is respectfully requested.

Preliminarily, Applicants note that claims 1-11 and 15-17 were rejected by the Examiner under "35 U.S.C. § 102(b) as being anticipated by [Matsuo et al.] (U.S. Pat. No. 6,236,385)." Applicant respectfully submits, however, that the Matsuo et al. is designated by U.S. Pat. No. 4,319,237 while Nomura et al. is designated by U.S. Pat. No. 6,236,385. For purposes of prosecution, and in view of the actual rejection of the aforementioned claims, Applicants hereby assume the Examiner intended to reject claims 1-11 and 15-17 under 35 U.S.C. § 102(b) as being anticipated by Matsuo et al.

Claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, "...resetting each liquid crystal cell of the liquid crystal

display device simultaneously." None of the cited references, including Matsuo et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 1 and claims 2 and 3, which depend therefrom are allowable over the cited references.

The Examiner cites Matsuo et al. as teaching "...resetting each liquid crystal cell of the liquid crystal display device simultaneously (col. 4, lines 27-40)."

Applicants respectfully submit, however, Matsuo et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 1. For example, Applicants respectfully submit Matsuo et al. states at column 4, lines 36-40 "By using the period of 5 ms at the end of each frame, the reset signal source 32 sequentially applies reset signals to the capacitors, through the electrode lines 29 and the diodes 23 thereby to reset the capacitors 27 to zero level." Accordingly, Applicants respectfully submit Matsuo et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 1.

Claim 4 is allowable over the cited references in that claim 4 recites a combination of elements including, for example, "wherein a reset voltage is applied to all liquid crystal cells of the liquid crystal display device to reset the liquid crystal display device". None of the cited references, including Matsuo et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 4 and claims 5-8, which depend therefrom are allowable over the cited references.

The Examiner cites Matsuo et al. as showing "wherein a reset voltage is applied to all liquid crystal cells of the liquid crystal display device to reset the liquid crystal display device (col. 4, lines 27-40)."

Applicants respectfully submit, however, Matsuo et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 4. For example, Applicants respectfully submit Matsuo et al. states at column 4, lines 27-40 For example, Applicants respectfully submit Matsuo et al. states at column 4, lines 37-40 "...the reset signal source 32 sequentially applies reset signals to the capacitors, through the electrode lines 29 and the diodes 23 thereby to reset the capacitors 27 to zero level." Accordingly, Applicants respectfully submit Matsuo et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 4.

In rejecting claims 5 and 6, the Examiner cited Matsuo et al. as teaching "wherein the reset voltage is applied to a common electrode of the liquid crystal display device, and wherein the reset voltage applied to the common electrode is less than a common voltage applied to the common electrode in a data charging interval (col. 8, lines 56 through column 9, line 23; fig. 13; column 8, lines 47-67).

Applicants respectfully submit, however, that the "reset voltage", cited by the Examiner has being taught by Matsuo et al. in rejecting claim 4 is disclosed with reference to Figure 7 of Matsuo et al. Figure 7 of Matsuo et al. describes a Prior Art embodiment while column 8, line 47 – column 9, line 23 of Matsuo et al. describes an embodiment of Matsuo et al. illustrated in Figure 13 where the application of a "reset voltage", such as that of Figure 7, is absent. Accordingly, Applicants respectfully submit that Matsuo et al. does not teach or suggest at least the aforementioned combination of elements.

In rejecting claims 7 and 8, the Examiner stated "[claims 7 and 8] ...have substantially the same limitations of claim 3. Therefore, they are analyzed as previously discussed in claim 3 above." Contrary to the Examiner's statement, Applicants respectfully submit that at least claim 8 does not include limitations found in claim 3.

Claim 9 is allowable over the cited references in that claim 9 recites a combination of elements including, for example, "A reset circuit for a liquid crystal display device, comprising: voltage selecting means for selecting...a normal common voltage to be applied... in an interval when a data voltage is charged and maintained in all liquid crystal cells of the liquid crystal display, and for selecting... a reset voltage less than the normal common voltage to be applied to the common electrode in a reset interval." None of the cited references, including Matsuo et al., singly or in combination, teaches or suggests at least these features of the claimed invention.

In rejecting claim 9, the Examiner stated "[claim 9] ...has substantially the same limitations of claims 1-3. Therefore, they are analyzed as previously discussed in claims 1-3 above." Contrary to the Examiner's statement, Applicants respectfully submit that limitations found in claim 9 are not found in claim 3.

Claim 10 is allowable over the cited references in that claim 10 recites a combination of elements including, for example, "a voltage amplifier for amplifying an input control signal having a specific logical state only in a reset interval when liquid crystal cells of the liquid crystal display device are reset..." None of the cited references, including Matsuo et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 10 and claim 11, which depends therefrom are allowable over the cited references.

The Examiner cites Matsuo et al. as showing "a reset circuit... comprising[:] a voltage amplifier (not the voltage applied to input 54 is amplified by transistor 60) for applying an input control signal having a specific logical state only in a reset interval ...(col. 10, lines 3-10).

Applicants respectfully submit, however, that Matsuo teaches at column 10, lines 3-10 "...the erasing AC signal applied to the input terminal is amplified by the transistor 60." Accordingly, Applicants respectfully submit that Matsuo et al. does not teach or suggest at least the aforementioned combination of elements.

Claim 15 is allowable over the cited references in that claim 15 recites a combination of elements including, for example, "means for simultaneously resetting all of the liquid crystal cells". None of the cited references, including Matsuo et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Similar arguments presented above with respect to claims 1 are also applicable with respect to claim 15. Accordingly, Applicant respectfully submits that independent claim 15 and claims 16 and 17, which depend therefrom are allowable over the cited references.

The rejection of claims 12-14 under 35 U.S.C. § 103(a) as being unpatentable over Matsuo et al. in view of Berting et al. (U.S. Pat. No. 4,393,379) is respectfully traversed and reconsideration is respectfully requested.

Preliminarily, Applicants note that claims 12-14 were rejected by the Examiner under "35 U.S.C. § 103(a) as being unpatentable over [Matsuo et al.] in view of [Berting et al.]. In the body of the rejection "Nomura" was used to as the primary reference while Matsuo et al. was used as the secondary reference. For purposes of prosecution, and in view of the actual rejection of the aforementioned claims, Applicants hereby assume the Examiner intended to

use Matsuo et al. as the primary reference while using Berting et al. as the secondary reference.

Claim 12 is allowable over the cited references in that claim 12 recites a combination of elements including, for example, "logical OR gates for performing a logical OR operation of an input reset signal and each gate driving signal from the shift register". None of the cited references, including Matsuo et al. or Berting et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 12 and claims 13 and 14, which depend therefrom are allowable over the cited references.

The Examiner cites Matsuo et al. as teaching "a reset circuit for a liquid crystal display device" and acknowledges that "[Matsuo et al.] fail to teach about a shift register, logical OR gates for performing a logical OR operation of an input reset signal and each gate driving signal from the shift register..." The Examiner then cites Berting et al. as teaching the limitations that were not disclosed by Matsuo et al., citing to Figures 1 and 2 and column 2, line 55 – column 3, line 4 of Berting et al. Lastly, the Examiner concludes that "it would have been obvious to... improve upon the non-multiplexed LCD drive circuit, as disclosed by [Berting et al.]. Doing so would provide a low cost LCD drive circuit that is suitable for instrumentation applications."

Applicants respectfully submit, however, that Berting et al. teaches at column 2, line 55 – column 3, line 4 "Shift register 14 is of conventional type having a number of parallel output terminals 11 corresponding to the number of LCD electrical lines to be driven. The shift register 14 could, for example, comprise a number of tandomly connected four bit static shift registers... parallel output lines 11_1-11_n, a serial input terminal 13a and a serial output

terminal 13b. ...The contents of the shift register 14 are reset or cleared by application of a logic zero signal to CLEAR terminal 19." Accordingly, Applicants respectfully submit that neither Matsuo et al. nor Berting et al., either singly or in common, teach or suggest at least the aforementioned combination of elements. Further, Applicants respectfully submit Berting et al. is directed to "non-multiplexed LCD driver circuitry have data update and refresh capabilities." (see Berting et al., column 1, lines 6-7) Accordingly, Applicants respectfully submit the Examiner's aforementioned conclusion "it would have been obvious to... improve upon the non-multiplexed LCD drive circuit, as disclosed by [Berting et al.]. Doing so would provide a low cost LCD drive circuit that is suitable for instrumentation applications" does not provide any motivation to modify Matsuo et al. with Berting et al.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136. Please credit any overpayment to deposit Account No. 50-0911.

Respectfully submitted,

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MARKED UP VERSION OF THE AMENDED CLAIM

8. (AMENDED) The method as claimed in claim [7] 4, wherein the reset voltage is a gate high voltage simultaneously applied to the gate electrode lines of the liquid crystal display device.